We claim:

1. An electrically addressable data storage unit having a plurality of data storage arrays on a substrate, each array having a matrix of coplanar data storage cells connected by row lines and column lines for recording, addressing and reading of data, comprising:

(a) a plurality of row address lines, each row address line being in electrical communication with the rows of predetermined multiple arrays within the data storage arrays on the substrate,

(b) a plurality of column address lines, each column address line being in electrical communication with the columns of predetermined multiple arrays within the data storage arrays on the substrate,

(c) a plurality of power lines each being separately connected to one of the multiple arrays, and

(d) a controller connected to the plurality of row address lines, plurality of column address lines and plurality of power lines to selectively provide power to a selected array of the multiple arrays, to selectively address a row of data storage cells in the selected array and to selectively address a column of data storage cells in selected array, to thereby select a data storage cell in the selected array of the multiple arrays.

2. The data storage unit of claim 1, wherein the plurality of row address lines comprises a plurality of sets of row address lines, each set of row address lines being in electrical communication with the rows of more than one array.

3. The data storage unit of claim 1, wherein the plurality of column address lines comprises a plurality of sets of column address lines, each set of column address lines being in electrical communication with the columns of more than one array.

4. The data storage unit of claim 1, wherein the plurality of data storage arrays are arranged in a matrix of rows and columns.

5. The data storage unit of claim 4, wherein each row address line is in electrical communication with the rows of all of the arrays in one column of arrays.

6. The data storage unit of claim 4, wherein each column address line is in electrical communication with the columns of all of the arrays in one row of arrays.

7. The data storage unit of claim 1, wherein each array includes row decoders in contact with the row lines and column decoders in contact with the column lines.

8. The data storage unit of claim 7, wherein each row address line is in contact with the row decoders of the multiple arrays and each column address line is in contact with the column decoders of the multiple arrays.

9. The data storage unit of claim 1, wherein the controller is disposed to select values for the row and column power lines of all arrays other than the selected array to turn off all data storage cells in the other arrays.

10. The data storage unit of claim 9, wherein the controller is disposed to select values for the row and column power lines of all arrays other than the selected array so as to match voltages on the rows and columns of the unselected arrays, to thereby turn off all data storage cells in the unselected arrays without reverse biasing said data storage cells.

11. The data storage unit of claim 1, and further comprising a plurality of row power lines for each of the multiple arrays, each row power line being connected to a portion of the rows in one of the multiple arrays, and a plurality of column power lines for each of the multiple arrays, each column power line being connected to a portion of the columns in one of the multiple arrays.

12. The data storage unit of claim 1, and further comprising a sense line connected to the selected array, having a voltage to detect the value of the selected data cell during a read cycle.

13. The data storage unit of claim 1, wherein the controller is disposed to apply voltages to the selected cell that are sufficient to change the value of the selected cell during a write cycle.

14. The data storage unit of claim 1, and further comprising an inhibit line connected to the selected cell having a voltage to turn off the selected cell during a write cycle.

15. An electrically addressable data storage unit having a plurality of data storage arrays on a substrate, each array having multiple coplanar data storage cells for recording, addressing and reading of data, comprising a plurality of address lines, each address line being in common with predetermined multiple arrays on the substrate.

16. The data storage unit of claim 15, wherein the plurality of address lines comprises a plurality of row address lines, each row address line being in common with the rows of predetermined multiple arrays on the substrate.

17. The data storage unit of claim 15, wherein the plurality of address lines comprises a plurality of column address lines, each column address line being in common with the columns of predetermined multiple arrays on the substrate.

18. The data storage unit of claim 15 and further comprising a plurality of power lines each being separately connected to one of the multiple arrays.

19. The data storage unit of claim 18 and further comprising a controller connected to the plurality of power lines and address lines to selectively address a data storage cell in a selected array while turning off the data storage cells in all unselected arrays.

20. The data storage unit of claim 19, wherein the controller provides voltage values on the plurality of power lines to provide matching voltages on the rows and columns of all unselected arrays, thereby turning off all unselected cells in the unselected arrays without reverse biasing the unselected cells.

21. A method for recording, addressing and reading of data in an electrically addressable data storage unit having a plurality of data storage arrays, each array having a matrix of coplanar data storage cells connected by row lines and column lines, comprising:

(a) connecting a plurality of row address lines in electrical communication with prerdetermined multiple arrays within the plurality of arrays, each row address line being in electrical communication with selected rows of the predetermined multiple arrays to selectively address a row of data storage cells in a selected array of the predetermined multiple arrays,

(b) connecting a plurality of column address lines in electrical communication with predetermined multiple arrays within the plurality of arrays, each column address line being in electrical communication with selected columns of the predetermined multiple arrays to selectively address a column of data storage cells in the selected array of the predetermined multiple arrays,

(c) connecting a plurality of power lines to the plurality of arrays, each power line being separately connected to one of the multiple arrays to selectively provide power to the data storage cells of the selected array, and

(d) selectively addressing a data storage cell in said one array through a controller connected to the plurality of power lines, plurality of row address lines and plurality of column address lines.

22. The method of claim 21, wherein the plurality of data storage arrays are arranged in a matrix of rows and columns, and further comprising placing each row address line in electrical communication with the rows of each array in a column of the matrix of arrays, and placing each column address line in electrical communication with the columns of each array in a row of the matrix of arrays.

23. The method of claim 21, and further comprising providing power to the plurality of arrays with a row power line and a column power line for each array by connecting the row power line to the rows of said each array and connecting the column power line to the columns in said each array.

24. The method of claim 23, wherein the step of providing power to the selected array comprises providing power values to the row and column power lines of the selected array so as to enable the selected data storage cell in the selected array.

25. The method of claim 23, wherein the step of providing power to the plurality of arrays comprises providing power to the rows and columns of each unselected array so that the row voltages match the column voltages, thereby turning off all memory cells in the unselected arrays to disable all data storage cells in the unselected arrays without reverse biasing said storage cells.

26. The method of claim 21, and further comprising connecting a plurality of sense lines to each of the plurality of arrays and providing a voltage to the sense line connected to the selected array to sense the value of the selected data storage cell.

27. The method of claim 21, wherein each data storage cell comprises a diode, and wherein the diode of the selected data storage cell is forward biased.

28. The method of claim 27, wherein the row and column voltages on the plurality of arrays other than said one array are matched so that the memory cells in the unselected arrays are turn off without being reversed biased, thereby eliminating leakage current from the unselected arrays.

29. A method for recording, addressing and reading of data in an electrically addressable data storage unit having a plurality of data storage arrays, each array having a plurality of coplanar data storage cells, comprising connecting a plurality of address lines so that each address line is in common with predetermined multiple arrays on the substrate.

30. The method of claim 29 wherein the step of connecting the plurality of address lines comprises connecting a plurality of row address lines so that each row address line is in common with a column of the predetermined multiple arrays on the substrate.

31. The method of claim 29 wherein the step of connecting the plurality of address lines comprises connecting a plurality of column address lines so that each column address line is in common with a row of the predetermined multiple arrays on the substrates.

32. The method of claim 29 and further comprising connecting a plurality of power lines so that each power line is separately connected to one of the multiple arrays.

33. The method of claim 32 and further comprising connecting a controller to the plurality of power lines and address lines to selectively address a data storage cell in a selected array while turning off the data storage cells in all unselected arrays.

34. The method of claim 33 wherein the step of connecting the controller comprises providing matching voltages on rows and columns of unselected arrays, to turn off the memory cells in unselected arrays without reverse biasing said memory cells, thereby minimizing the amount of leakage current in the unselected arrays.